WE CLAIM:

1. An integrated circuit located between isolation trenches at the surface of a semiconductor, comprising:

    a first well of a first conductivity type having a first resistivity;

    said first well having a shallow buried region of higher resistivity than said first resistivity, said region extending between said isolation trenches;

    a second well of the opposite conductivity type extending to said surface between said isolation trenches, having a contact region and forming a junction with said shallow buried region of said first well, substantially parallel to said surface; and

    a MOS transistor located in said second well, spaced from said contact region, and having source, gate and drain regions at said surface, wherein said space is predetermined to create a small voltage drop in I/O transistors for conditioning signals and power to a pad, or large voltage drops in ESD circuits for protecting the active circuitry connected to a pad.

2. The circuit according to Claim 1 wherein said space is configured in linear or meandering or any other suitable outline.

3. The circuit according to Claim 1 wherein said space includes a dummy gate or an isolation region or an otherwise protected surface.

4. The circuit according to Claim 3 wherein said junction

varies in distance to said surface in accordance with the configuration of said transistor gate and dummy gate structures, or isolation region.

5. The circuit according to Claim 1 further comprising an additional well of the first conductivity type electrically in series with said well of the opposite conductivity type so that the sum of their electrical resistances provides the large voltage drop in ESD applications required for protecting the active circuitry connected to said pad.

6. The circuit according to Claim 1 wherein said semiconductor chip is made from a material selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material used in integrated circuit fabrication.

7. The circuit according to Claim 1 wherein said first conductivity type is n-type and the semiconductor has a dopant species selected from a group consisting of arsenic, phosphorus, antimony, and bismuth.

8. The circuit according to Claim 1 wherein said region of higher resistivity may have a resistivity about an order of magnitude higher than said first resistivity, where said higher resistivity is brought about by a compensating doping process, which uses, for an n-type first conductivity, a dopant species selected from a group consisting of boron, aluminum, gallium, indium, and lithium.

9. The circuit according to Claim 1 further comprising:

an electrical connection of said source to Vss (ground) potential;

an electrical connection of said drain to said pad potential;

an electrical connection of said contact region to Vss (ground) potential;

an electrical connection of said first well to Vdd potential;

an operation of said MOS transistor such that a voltage drop is caused by the part of the drain avalanche current flowing to said contact region through the resistance of said second well;

whereby, when said resistance is small, said voltage drop conditions signal and power to said pad; and

whereby, when said resistance is large, said voltage drop de-biases said junction between said second well and said low-doped portion of the first well, turning-on the lateral transistor formed by drain, second well, and contact, and enhancing the ESD protection of said pad.

10. The circuit according to Claim 9 wherein said Vdd potential is positive.

11. The circuit according to Claim 9 wherein, under ESD conditions, said pad potential is positive and said drain avalanche flow comprises holes.

12. A method for fabricating an integrated circuit located between isolation trenches at the surface of a semiconductor chip for, comprising the steps of:

depositing a first photoresist layer over said chip surface and opening a window in said first layer between first isolation regions in said surface;

implanting, at high energy and high dose, ions of a first conductivity type into said surface through said window, creating a first well of a first conductivity type;

removing said first photoresist layer;

depositing a second photoresist layer over said chip surface and opening a window in said second layer between second isolation regions in said surface, said second isolation regions nested within said first isolation regions;

implanting, at high energy and low dose, ions of the opposite conductivity type into said surface through said window, creating, by partial doping compensation, a region of lower doping concentration of the first conductivity type embedded in said first well, resulting in a regional resistivity higher than the resistivity of the first well;

removing said second photoresist layer;

forming the gate structures for a MOS transistor positioned in the surface space between said second isolation regions;

depositing a third photoresist layer over said chip surface and opening a window in said third layer between said second isolation regions in said surface;

implanting, at medium energy and medium dose, ions of the opposite conductivity type into said surface through said window and through said gate structures, creating a second well of opposite conductivity type close to and substantially parallel to said surface;

implanting, at low energy and high dose, ions of the first conductivity type into said surface through said window, creating the drain extension regions of said MOS transistor;

implanting, at low energy and low dose, ions of the

opposite conductivity type into said surface through said window and through said gate structures, adjusting the gate voltage Vt of said MOS transistor;

removing said third photoresist layer;

forming insulating sidewalls on said gate, deep source and drain regions of said MOS transistor, and contact region of said second well, whereby said contact region is spaced from said MOS transistor by a predetermined distance.

13. The method according to Claim 12 wherein said predetermined distance is selected to create a small voltage drop in I/O transistors for conditioning signals and power to a pad.

14. The method according to Claim 12 wherein said predetermined distance is selected to create a large voltage drop in ESD circuits for protecting the active circuitry connected to a pad.

15. The method according to Claim 12 further comprising the step of:

forming dummy gate structures concurrently with forming said MOS transistor gate structures;

thereby modulating the distribution of the subsequently implanted ions so that the junction between said second well and said region of higher first-well resistivity varies in distance to said surface in accordance with the configuration of said transistor gate and dummy gate structures.

16. The method according to Claim 12, wherein said step of

implanting ions of the opposite conductivity type at medium energy and medium dose is replaced by the step of implanting ions of the opposite conductivity type at medium-to-high energy and medium dose.

17. The method according to Claim 16, after the step of forming the gate structures further comprising the step of:

forming an isolation region at said surface, extending between said MOS transistor source region and said second-well contact region;

thereby modulating the distribution of the subsequently implanted ions so that the junction between said second well and said region of higher first-well resistivity varies in distance to said surface in accordance with the configuration of said isolation region and said transistor gate structure.

18. The method according to Claim 12 further comprising the step of annealing said high energy implant at elevated temperature.

19. The method according to Claim 12 wherein said implanting of medium energy ions comprises ions having an energy suitable for creating the second-well junction at depth between 200 and 400 nm, and a peak concentration from about 5 · 10E17 to 5 · 10E20 cm-3.

20. The method according to Claim 17 wherein said implanting of medium-to-high energy ions comprises ions having an energy suitable for creating the second-well junction at a depth between 600 and 800 nm, and a peak concentration from about 5 · 10E19 to 5 · 10E20 cm-3.

21. The method according to Claim 12 wherein said implanting of high energy ions comprises ions having an

energy suitable for creating the first well and the partially compensated region at a depth between 900 and 1100 nm.